Appendix B.

Radar Timing Generator Description (RTG)

1. INTRODUCTION

The Radar Timing Generator (RTG) resides on a single VME card, and generates all the repetitive signals necessary to trigger the radar, control data acquisition, control transmit and receive polarization, and drive A-scope displays. All timing parameters are programmable from the VME bus.

2. OVERVIEW

2.1 Programmers' Model

All programmable parameters are available on the VME bus in 16-bit words, although mostly the lower order bits are used. VME addressing is big-endian, and so the most significant byte (even address) is addressed. Before changing parameters, the Run Enable bit in the overall control word should be cleared. This causes all counting to stop, and loads all counters with the values in their associated hold registers. When the Run bit sets, counters are allowed to run, and radar triggers and range gates start.

The RTG is divided into five functions: Overall Controller, Radar Trigger Generator, Range Gate Generator, Transmitter Controller and Polarization Controller. Each of these functions has a group of 16 byte addresses, or eight word addresses, reserved for it.

The Overall Controller function controls the VME function of interrupt control, as well as internal/external clock selection for timing.

The Radar Trigger Generator controls the spacing between Radar Triggers (RTs), the delay between the first trigger (RT1) and the second trigger (RT2) in double pulse mode, the number of triggers in a beam, and the number of triggers between beams.

The Range Gate Generator controls the delay from RT to the first range gate, the range gate spacing, and the number of range gates in the block.

The Transmitter Controller controls the spacing of the two pre-triggers, and the length of the radar trigger.

The Polarization Controller controls transmitter and receiver polarization.

2.2 Signal Model

The RTG can either be a master, in which case it generates all timing from an on-board 20 MHz clock, or a slave, in which case it receives an external 16 MHz clock, external radar triggers, and an external sync signal.

Timing begins with an external 16 MHz clock or an on-board 20 MHz clock. A program-controlled bit selects which clock to use. The selected clock is divided down to 1 MHz and used to generate radar triggers. This 1 MHz clock is used to generate all timing parameters except for the range gate spacing. After Run is set, there is a delay of PRPR before the first RT1 occurs. The first trigger generated is actually the first occurring pre-trigger: PRT1B. The next pre-trigger, PRT1A, is generated as a delay from PRT1B, as is RT1. PRT1B also starts the RT2 counter, which generates PRT2B. PRT2A and RT2 are generated as delays from PRT2B. The correspondingly delayed triggers are ORed together to produce composite triggers RTB, RTA, and RTint. RTint is the same trigger that is eventually sent to the pulse modulator, RT, except that RT goes through a circuit that allows its length to be programmed. All triggers except for RT are one clock period long.

Triggers are counted in two ways: in a beam counter, which counts the number of RT1s in a beam (NTRG); and in a wait counter, which counts the number of RT1s to wait between beams (NPWT). These counters have no effect on the actual triggering of the radar, but rather serve to slow down data acquisition by inhibiting range gates during the wait period by use of signal RGinh. A Beam signal is also produced at prt1b time that marks the beginning of data acquisition for the beam. A MidBeam signal is also generated that generates a VME interrupt.

RT1 and RT2 presently drive a single range gate generator that produces blocks of range gates following each trigger. Future enhancements may generate two blocks of range gates, the first of which may overlap RT2. Software must still insure that the two blocks of range gates do not overlap each other.

3. FUNCTIONS WITHIN THE RTG

3.1 Overall Control

Interrupt control is here, including bits to enable interrupts and a programmable interrupt vector. Also the internal/external clock select and the Run control are programmed here.

The Run Enable bit should be turned off whenever other registers are being updated. When Run Enable is set, Run will either set immediately or will wait for an external sync signal before setting, depending on the setting of the External Sync Enable bit. Internally generated radar triggers will begin one PRPR period after Run sets. Externally generated radar triggers may begin at any time, depending on the timing of the master trigger generator.

3.2 Radar Trigger Generator

The RT Generator function is contained on one EPLD (trig_gen) which runs from a 1 MHz clock. The RTG generates radar triggers in a double pulse mode. The two triggers (RT1 & RT2) each have a variable range gate block following them. Single-trigger mode works the same as double-trigger mode except that RT2 is turned off.

3.3 Range Gate Generator

The RG Generator function is contained on one EPLD (gate_gen) which runs from a 20 MHz local clock, or a 16 MHz external clock.

Data acquisition on the ICS-150 board is controlled by two external signals: RG0 and RGclk. Other parameters are programmable via the VME bus in the ICS-150 itself. These parameters include the number of range gates and a decimation value. The board must receive a continuous clock at the range gate rate, RGclk. To start data acquisition, it then must receive a signal, RG0, before the first range gate. When it receives RG0, the first range gate will occur at the next RGclk edge following. It will then acquire the number of range gates programmed into it, which may vary from 128 to 8192 in powers of two. The RGclk may only vary from 3.75 MHz to 20 MHz, and so a decimation register is provided to allow slower sampling. This register may be programmed from 1 to 256.

In operation, the RTG supplies a continuous 20 MHz clock for RGclk, and the decimation register is used to set the range gate spacing. This means that the spacing can be set in multiples of 50 ns. Therefore, the only RTG parameter that actually controls the data-acquisition process is the range gate delay. Everything else is controlled by the programming of the ICS-150.

It is desirable, however, to be able to view range gates on an A-scope or PPI and so range gates are generated that mirror the ICS-150's internal sampling pulses. For this reason, there are additional registers for range gate spacing and number of range gates. Note that although any number of range gates may be set for the A-scope display, the ICS150 only generates gates in powers of two. This means that the ICS150's gates may overlap RT2, although the gates shown on the A-scope do not overlap. If this occurs, data acquisition slows dramatically because no gates are generated following RT2.

The range gate delay is controlled in steps of 1 µs. The range gate spacing is controlled in steps of one clock period (either 50 ns or 62.5 ns), up to 256 clock periods (either 12.8 µs or 16 µs). The number of range gates can be programmed from 1 to 16384.

3.4 Transmitter

The Transmitter function controls the pre-trigger delays, and the length of the radar trigger, which may be programmed in increments of one clock period.

3.5 Polarization Control

There are two eight-bit registers: one for transmit polarization and one for receive polarization. A 0 signifies horizontal polarization and a 1 signifies vertical polarization. The MSB is the first polarization at the beginning of the beam. In single-trigger mode, each RT1 shifts out a bit; in-double trigger mode, RT1 and RT2 both shift out a bit. The shift register is arranged as a circular shift register and shifting continues until the beam is finished. At the beginning of a beam, the register is initialized to the starting pattern so that all beams have identical polarization.

4. EPLD PARTITIONING

The logic for the RTG is portioned into three EPLDs, as described below.

4.1 vme_xmit

This EPLD contains VME functions and the Transmitter Controller.

4.2 trig_gen

This EPLD contains the Radar Trigger Generator and the Polarization Controller.

4.3 gate_gen

This EPLD contains the Range Gate Generator and the Overall Controller.

5. RTG ADDRESS SPACE

All addressable registers on the RTG1 board are 16 bits and are addressed using a 10-bit address, with the LSB of the address always zero. VME addressing is big-endian, so the even address indicates the most significant byte in a 16-bit word.

Table 1. Overall Address Assignment

Hex Address	Function
80-8F	Overall control
90-9F	Radar Trigger Generator
A0-AF	Unassigned
B0-BF	Range Gate Generator
C0-CF	Transmitter Control
D0-DF	Unassigned
E0-EF	Polarization Control
F0-FF	Unassigned
100-1FF	Unassigned

Table 2.Overall Controller

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x80 INTC	test bit				interrupt control	interrupt control*	green LED indicator	red LED indicator
Type	R/W				R/W	RO	WO	WO
=0	no function				interrupts disabled	no interrupt pending	green LED off	red LED on
=1	no function				interrupts enabled	interrupt pending	green LED on	red LED off
0x82 INTV	vector	vector	vector	vector	vector	vector	vector	vector
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x84 RTGC				16/20 MHz ext clk select	Run	Ext Sync Enable	Run Control	Clock Select
Type				WO	RO	WO	WO	WO
=0				20 MHz ext clk	Run false	don't wait for ext sync	don't Run	use local 20 MHz clock
=1				16 MHz ext clk	Run true	wait for ext sync	Run enabled	use external clock

*not implemented

Table 3. Radar Trigger Generator Addressing

Hex Address	Function	Abv	Bits	Format	Range
90|91	Control Word	RTCN	2		
92|93	Pulse Repetition Period in 1μsec increments	PRPR	14	2's comp	3 to 16384 μsec
94|95	Spacing between RT1 & RT2 in 1 μsec increments	TRGS	10	2's comp	2 to 1024 μsec
96|97	Number of RT1s in beam	NTRG	12	2's comp	2 to 4096
98|99					
9A|9B	Number of RT1s to wait between beams	NPWT	10	2's comp	0 to 1023
9C|9D					
9E|9F					

Table 4. Radar Trigger Control Word

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x90 RTCN					Skip RT*		Single/Double	Internal/ External
Type					WO		WO	WO
=0					don't skip		Single trigger	Internal triggers
=1					Skip RGs every other RT		Double trigger	External triggers

*not implemented

Table 5. Range Gate Generator Addressing

Hex Address	Function	Abv	Bits	Format	Range
B0|B1	Range Gate Control Word	RGCN	2		
B2|B3	Delay from RT to RGs in 1 μsec increments	DLAY	10	2's comp	2 to 1025 μsec
B4|B5	Spacing between range gates in 50 ns increments	SPAC	8	2's comp	1 to 256
B6|B7	Total number of range gates	NRGT	14	2's comp	1 to 16,384
B8|B9					
BA|BB					
BC|BD					
BE|BF					

Table 6. Range Gate Control Word

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xB0								RG enable
Type								WO
=0								No gates/end gates at beam
=1								Start gates at beam

Table 7. Transmitter Controller

Hex Address	Function	Abv	Bits	Format	Range
C0|C1	Transmitter Control Word*	TXCN			
C2|C3	Trigger B to Trigger A spacing	BASP	6	2's comp	1 to 63 μsec
C4|C5	Trigger B to RT spacing	B0SP	6	2's comp	2 to 63 μsec
C6|C7	Radar trigger length	RTLN	6	2's comp	1 to 64 ticks
C8|C9					
CA|CB					
CC|CD					
CE|CF					

*not implemented

Table 8. Transmitter Control Word

Hex Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xC0								
Type								
=0								
=1								

Table 9. Polarization Controller

Hex Address	Function	Abv	Bits	Range
E0|E1	Polarization Control Word*	PLCON		
E2|E3	Transmit Polarization Mode	XPOL	8	
E4|E5	Receive Polarization Mode	RPOL	8	
E6|E7				
E8|E9				
EA|EB				
EC|ED				
EE|EF				

*not implemented

H or h polarization is 0.
V or v polarization is 1.
MSB is the first polarization; LSB is the last.

6. RADAR TIMING GENERATOR CONNECTORS

The following general comments apply to all connectors, except J7 and J8.

1) All connectors are standard ribbon cable style on a 0.1″ grid.
2) Pin 1 and all even-numbered pins are grounded. Even-numbered pins are not shown.
3) All connectors are a different size.
4) All levels are standard TTL levels, unless noted.

Pin	Signal	I/O	Comment
1	GND	P	
3	RG_CLK	O	Clock at range gate rate
5	RG0	O	Range gate zero--precedes first range gate
7	BEAM	O	Start of Beam
9			
11	RUN	O	Start of Run
13	Spare	X	
15	Spare	X	
17	Spare	X	
19	Spare	X	

Jack 1. VME Chassis Connector (20 pin)

Pin	Signal	I/O	Comment
1	GND	P	
3	RT	O	Radar Trigger
5	PRTA	O	Immediately precedes RT
7	PRTB	O	Precedes PRTA
9	RT1	O	Radar Trigger 1
11	PRT1A	O	Immediately precedes RT1
13	PRT1B	O	Precedes PRT1A
15	RT2	O	Radar Trigger 2
17	PRT2A	O	Immediately precedes RT2
19	PRT2B	O	Precedes PRT2A
21	XMIT_POL	O	Transmitted polarization
23	RCV_POL	O	Received polarization
25	Spare	X	Reserved for other options
27	Spare	X	Reserved for other options
29	Spare	X	Reserved for other options
31	Spare	X	Reserved for other options
33	Spare	X	Reserved for other options

Jack 2. Receiver/Transmitter Connector (34 pin)

Pin	Signal	I/O	Comment
1	GND	P	
3	RT1	O	A-scope trigger
5	RG	O	Range gates for A-scope
7	RT1	O	A-scope trigger
9	RG	O	Range gates for A-scope
11	RT1	O	A-scope trigger
13	RG	O	Range gates
15	RT	O	Radar trigger
17	RG_CLK	O	Clock at fastest range gate rate (20 MHz or ext clk)
19	RG0	O	Range gate zero--precedes first range gate
21	BEAM	O	Start of Beam
23			
25	RUN	O	Start of run
27	XMIT_POL	O	Transmitted polarization
29	RCV_POL	O	Received polarization
31	Spare	X	
33	Spare	X	
35	Spare	X	
37	Spare	X	
39	arb_clk	O	Triggers ARB. Gives 2 pulses/RT that ARB needs.

Jack 4. Display Connector (40 pin)

Pin	Signal	I/O	Comment
1	GND	P	
3	P^3_CLK	I	P^3 Clock (16 MHz)
5	P^3_RT	I	P^3 radar trigger
7	P^3_PR	I	P^3 processor reset
9	Spare	X	

Jack 5. Slave Connector (10 pin)

Pin	Signal	I/O	Comment
24	GND	P	
26	RGCLK	O	20 MHz or external clock frequency

Jack 7. ICS150 A/D Connector (34 pin)

Pin	Signal	I/O	Comment
26	RG0	O	Precedes first range gate
28	GND	P	

Jack 8. ICS150 A/D Connector (34 pin)